

Chapter 1 Product Introduction

1.1 Main Info

MB-ix-7xxU motherboard is based on Intel KabyLake-U processors.

1.2 Specification

KabyLake-U processor:

i7-7500U, dual ore, 2.7GHz, supporting turbo frequency and EIST technology

i5-7200U, dual core, 2.5GHz, supporting turbo frequency and EIST technology;

i3-7100U, dual core, supporting EIST technology;

Celeron 3865U, dual core, 1.8GHz, supporting EIST technology.

Memory: 2*SO-DIMM DDR4 up to 32GB.

GPU: Integrated; 1*HDMI, 1*DP, 1*LVDS (can change to eDP); DP to HDMI converter optional.

Storage: 1*M.2 Key B (for 2242 SSD);

2*SATA3.0 (max.);

1*eMMC (optional).

USB: 4*USB3.0;

4*USB2.0.

Ethernet: 2*LAN (intel i211).

Audio: Onboard High resolution audio chip; supporting Speaker_out, MIC_in, SPDIF and amplifier.

I/O: 5*RS232, 1*RS485;

1*LPT by header;

1*PS/2 (KB/MS header).

Others: 1*M.2 Key B (supporting NGFF 3G/4G module);

1*M.2 Key E (supporting NGFF WIFI);

1*PCIE 4X;

8*GPIO.

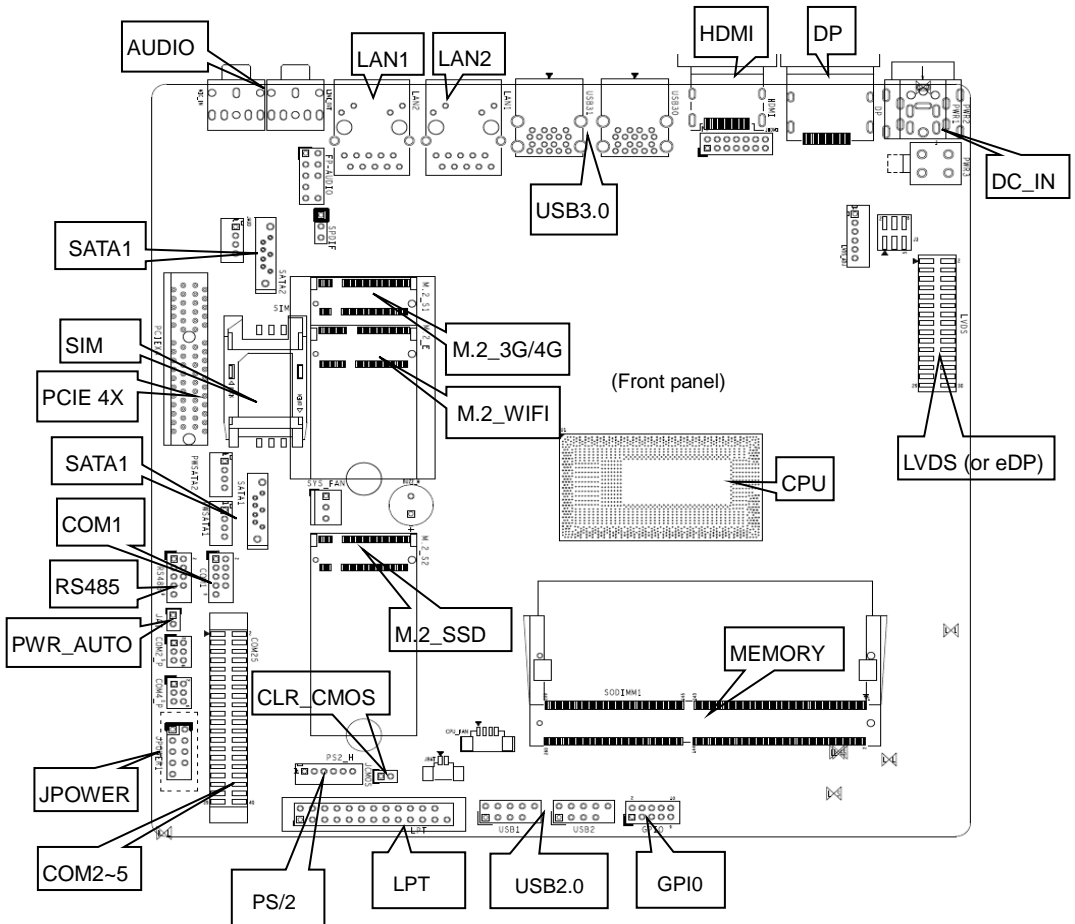
MB-i5-7200U-2L6C V1.1

Size: 170mm x 170mm

Power: 12V DC_IN adapter

Operating Temperature: -40°C-60°C

1.3 Diagram



MB-i5-7200U-2L6C Introduction

Chapter 2 Hardware

2.1 Jumper setting

Set jumpers according to your needs before installing hardware.

Tips about how to identify the first header of jumpers and interfaces: 1. Observe the mark beside plugs, the first header is usually marked by "1" or bold line or triangular symbol; 2. The first header is the square pad of pads on the back.

2.2 System Memory

Onboard 2*SO-DIMM DDR4-2133 slots up to 32GB memory.

2.3 Display interfaces

1*HDMI1.4 and one by header (cannot connect both at the same time), 1*DP1.2, 1*LVDS (can change to eDP1.3). Support trio independent display and 4K HD display.

2.4 LVDS (silk-print: LVDS, LVDS_ADJ, J3)

Dual channel 24bit LVDS. The power of LVDS screen cable is controlled by J3, and the backlight power is controlled by LVDS_ADJ.

LVDS:

Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

LVDS_ADJ:

MB-i5-7200U-2L6C Introduction

Pin	Signal
1	12V
2	12V
3	LCD_BKL_ON
4	LCD_BKL_ADJ
5	GND
6	GND

J3 (screen power jumper):

Interface	Setting	Function
1-2	Close	VCC(+3.3V)
3-4	Close	VCC(+5V)
5-6	Close	VCC(+12V)

Attention: LVDS screen's power can be adjusted from 12V/5V/3.3V via jumper setting. It is strictly forbidden to connect 2 or more interfaces via jumper cap at the same time.

2.5 eDP (silk-print: LVDS, LVDS_ADJ, J3)

This interface is optional, supporting 2 LANE eDP1.3. When this interface is onboard, LVDS does not work. The power of screen is controlled by J3 jumper, and the backlight power is controlled by LVDS_ADJ.

eDP header (silk-print: LVDS):

Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A
GND	25	26	GND
N/A	27	28	N/A

MB-i5-7200U-2L6C Introduction

N/A	29	30	N/A
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eDP backlight header (silk-print: LVDS_ADJ):

Pin	Signal
1	12V
2	12V
3	LCD_BKL_ON
4	LCD_BKL_ADJ
5	GND
6	GND

eDP voltage header (silk-print: J3):

Interface	Setting	Function
1-2	Close	VCC(+3.3V)
3-4	Close	VCC(+5V)
5-6	Close	VCC(+12V)

Attention: eDP screen's power can be adjusted from 12V/5V/3.3V via jumper setting. It is strictly forbidden to connect 2 or more interfaces via jumper cap at the same time.

2.6 HDMI header (silk-print: JHDMI)

HDMI header is reserved. HDMI port and header cannot be connected at the same time.

JHDMI:

Signal	Pin		Signal
DVI1_DATA2_P	1	2	DVI1_DATA2_N
DVI1_DATA1_P	3	4	DVI1_DATA1_N
DVI1_DATA0_P	5	6	DVI1_DATA0_N
DVI1_CLK_P	7	8	DVI1_CLK_N
DVI1_SCL	9	10	DVI1_SDA
VGA_DATA_5V	11	12	GND
DVI1_DETECT	13	14	GND

2.7 Expansion slots (silk-print: M.2_S1, M.2_E, PCIEX4)

M.2_S1: M.2 Key B for NGFF 3G/4G module, SIM slot onboard.

M.2_E: M.2 Key E for NGFF WIFI.

PCIEX4: for wifi card and video card.

MB-i5-7200U-2L6C Introduction

2.8 eMMC (silk-print: U8)

eMMC interface is optional and its capacity is also optional.

2.9 Storage interface (silk-print: SATA1, SATA2, M.2_S2)

Max. 2 SATA3.0 interfaces, and the speed is up to 6Gb/s. Onboard 2 SATA power sockets.

Only 1 SATA3.0 if Celeron processor onboard.

M.2_S2 is M.2 Key B for 2242 SSD.

2.10 USB (silk-print: USB1, USB2)

4*USB3.0 interfaces and 4*USB2.0 by header.

USB1, USB2:

Signal	Pin		Signal
VCC 5V	1	2	VCC 5V
USB DATA-	3	4	USB DATA-
USB DATA+	5	6	USB DATA+
GND	7	8	GND
(NC)	9	10	N/A

2.11 LAN

Intel i211 chip; 2*RJ45 interface; Supporting Magic packet wake-up and PXE.

LED indicator light:

LILED (orange)态	Function	ACTLED	Function
On	Connected	Flicker	Data transmission

2.12 Audio Interface (silk-print: FP_AUDIO, JAUD, SPDIF)

ALC662 audio control chip. The green one is Speaker-out, and the pink one is Mic-in; JAUD is amplifier output, and SPDIF header is SPDIF-out.

FP_AUDIO:

Signal	Pin		Signal
MIC2-L	1	2	AGND
MIC2-R	3	4	AVCC
FRO-R	5	6	MIC2-JD
F-IO-SEN(AGNG)	7	8	(NC)
FRO-L	9	10	LIN2-JD

MB-i5-7200U-2L6C Introduction

JAUD:

Pin	Signal
1	L+
2	L-
3	R-
4	R+

SPDIF:

Pin	Signal
1	+5V
2	SPDIF Out
3	GND

2.13 COM (silk-print: COM1, COM25, RS485, JCOM2_P, JCOM4_P)

6 COM. COM1 is industrial definition; COM2 supports RS232/RS422/RS485 via J4,J5 and J6 jumper setting. COM1, COM2, COM3, COM4 and COM5 is RS232, and COM6 is RS485. COM2_P and COM4_P provides 5V/12V (optional) voltage for COM2 and COM4.

COM1:

Signal	Pin		Signal
DCD#	1	2	DSR#
RXD	3	4	RTS#
TXD	5	6	CTS#
DTR#	7	8	RI#
GND	9	10	(NC)

COM25:

Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	10	N/A
DCD#	11	12	RXD
TXD	13	14	DTR#
GND	15	16	DSR#
RTS#	17	18	CTS#
RI#	19	20	N/A

MB-i5-7200U-2L6C Introduction

DCD#	21	22	RXD
TXD	23	24	DTR#
GND	25	26	DSR#
RTS#	27	28	CTS#
RI#	29	30	N/A
DCD#	31	32	RXD
TXD	33	34	DTR#
GND	35	36	DSR#
RTS#	37	38	CTS#
RI#	39	40	N/A

RS485:

Signal	Pin		Signal
DATA-	1	2	N/A
DATA+	3	4	N/A
N/A	5	6	N/A
N/A	7	8	N/A
GND	9	10	(NC)

COM2_P, COM4_P:

Interface	Setting	Function
1-2	Close	5V
3-4	Close	RI
5-6	Close	12V

2.14 LPT (silk-print: LPT)

Onboard 1*2X13PIN LPT interface. Pallets are a must for practical use. Customers can connect it to equipment like printer.

LPT:

Signal	Pin	
STB	1	2
LPT_ PPD0	3	4
LPT_ PPD1	5	6
LPT_ PPD2	7	8
LPT_ PPD3	9	10
LPT_ PPD4	11	12
LPT_ PPD5	13	14
LPT_ PPD6	15	16
LPT_ PPD7	17	18

MB-i5-7200U-2L6C Introduction

ACK	19	20
BUSY	21	22
PE	23	24
SLCT	25	26

2.15 GPIO (silk-print: GPIO)

Onboard 2×5Pin JGPIO header (2.0mm spacing), 8*GPIO input and output.

Signal		Pin	Signal
PCH_GPP_C16	1	2	3.3V
PCH_GPP_C17	3	4	PCH_GPP_A18
PCH_GPP_C18	5	6	PCH_GPP_A19
PCH_GPP_C19	7	8	PCH_GPP_A20
GND	9	10	PCH_GPP_A21

2.16 PS/2 (silk-print: PS2_H)

Onboard 6 pin PS/2.

Pin	Signal
1	+5V
2	KB_DATA
3	KB_CLK
4	MS_DATA
5	MS_CLK
6	GND

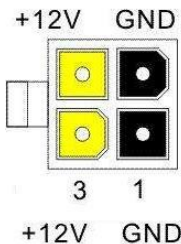
2.17 Motherboard power (silk-print: PWR1, PWR3)

12V DC_IN adapter or ATX12V (2x2PIN) power.

PWR1: 12V DC_IN adapter jack



PWR3: ATX12V (2x2PIN) power interface



2.18 Switch panel header (silk-print: JPOWER1)

Front panel interface is to connect function buttons and indicator lights on the case.

JPOWER1:

Signal	Pin		Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
RSTBTN+	5	6	PWR_ON+
RSTBTN-	7	8	PWR_ON-
N/A	9	10	(NC)

2.19 Auto power on (silk-print: JAT)

JAT:

Setting	JAT
Close	Auto power on

Attention: This jumper functions like "Restore AC Power Loss" on BIOS, and if the latter is set to be "Power on", this function will automatically work.

2.20 CMOS (silk-print: JCMOS)

CMOS is powered by the button battery on the board. Clearing CMOS will permanently clear previous system setting and restore it to factory setting.

Steps: 1. Turn the computer off and disconnect power;

2. Connect the jumper cap to THE 1ST and 2nd pin of JCMOS pin for 10 secs, and disconnect;

3. Turn the computer on, and press to enter BIOS setting, overload the best default value;

4. Save and exit.

JCOMS:

Setting	JCMOS
Close	Clear CMOS content



Don't clear COMS when the computer is connected to power to avoid damage to the board.